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Rapid manufacturing of low-noise membranes for nanopore sensors by *trans*-chip illumination lithography

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Abstract
In recent years, the concept of nanopore sensing has matured from a proof-of-principle method to a widespread, versatile technique for the study of biomolecular properties and interactions. While traditional nanopore devices based on a nanopore in a single layer membrane supported on a silicon chip can be rapidly fabricated using standard microfabrication methods, chips with additional insulating layers beyond the membrane region can provide significantly lower noise levels, but at the expense of requiring more costly and time-consuming fabrication steps. Here we present a novel fabrication protocol that overcomes this issue by enabling rapid and reproducible manufacturing of low-noise membranes for nanopore experiments. The fabrication protocol, termed *trans*-chip illumination lithography, is based on illuminating a membrane-containing wafer from its backside such that a photoresist (applied on the wafer's top side) is exposed exclusively in the membrane regions. *Trans*-chip illumination lithography permits the local modification of membrane regions and hence the fabrication of nanopore chips containing locally patterned insulating layers. This is achieved while maintaining a well-defined area containing a single thin membrane for nanopore drilling. The *trans*-chip illumination lithography method achieves this without relying on separate masks, thereby eliminating time-consuming alignment steps as well as the need for a mask aligner. Using the presented approach, we demonstrate rapid and reproducible fabrication of nanopore chips that contain small (12 μm $\times$ 12 μm) free-standing silicon nitride membranes surrounded by insulating layers. The electrical noise characteristics of these nanopore chips are shown to be superior to those of simpler designs without insulating layers and comparable in quality to more complex designs that are more challenging to fabricate.

(Some figures may appear in colour only in the online journal)

1. Introduction

Like their biological counterparts [8], solid-state nanopores [13, 14, 23, 24] represent a versatile single-molecule technique with which to investigate molecular properties of biomolecules [28, 27, 30] and biomolecular interactions [29, 31, 10]. The nanopore sensing concept utilizes chips (typically made in silicon (Si), figure 1(a)) that contain a thin free-standing membrane into which a nanometer-sized aperture (nanopore) is drilled (figure 1(b)) [26, 9, 13–15, 23, 30]. When a nanopore chip is placed in a saline solution and an electric potential is applied across the membrane, the ionic current will be determined by the possibility for ions to move through the nanopore. If a biomolecule, e.g. DNA, RNA, or a protein, moves through the nanopore [14], the ionic current will be partially blocked (figure 1(c)) [10, 13, 24]. In this way, individual molecules can be detected electrically. The concept is commonly used to investigate charged molecules,

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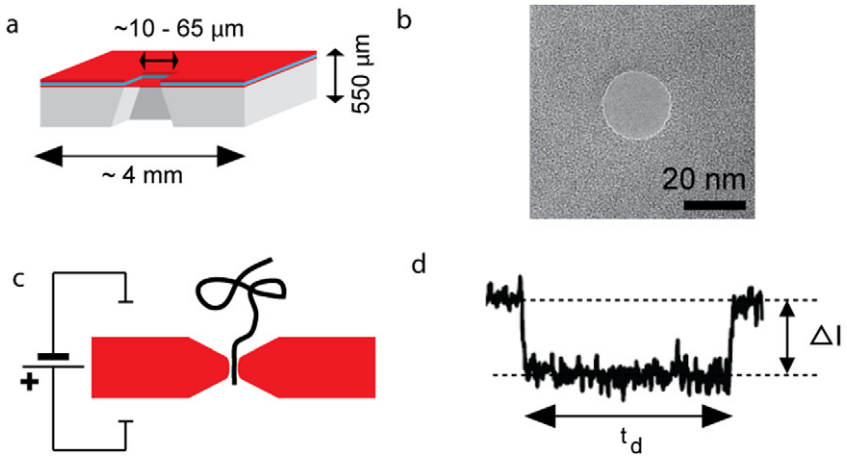

Figure 1. Molecular detection in nanopore experiments. (a) Schematic representation (vertical cross section) of a chip used in solid-state nanopore experiments [9, 13, 14, 25, 30]. The millimeter-sized silicon chip (gray) contains a micrometer-sized free-standing membrane (bottom red layer) in which a nanometer-sized hole (nanopore) is drilled. The area around the free-standing membrane is coated with insulating layers (top red and blue layer) to minimize electrical noise in the nanopore experiment. (b) Transmission electron microscope (TEM) image of a 20 nm wide nanopore drilled in a 20 nm thick free-standing SiN membrane. (c) Schematic representation of a typical nanopore experiment. The membrane (red) divides a reservoir containing a saline solution into two compartments. Each compartment is equipped with an electrode that allows one to control the electrical potential across the membrane, resulting in an ionic current through the nanopore. (d) When a molecule (black line in panel (c)) passes through the nanopore, the molecule partially blocks the ionic current due to volume exclusion. The depth of the current blockade (ΔI) and the dwell time (t_d) are characteristic respectively for the length and the diameter of the molecule [24].

which can be drawn through the pore electrophoretically by the same electric potential that is used to measure the ionic pore current [10, 13, 21, 28–30]. Apart from the possibility to detect single molecules, the concept provides information on molecular length, size, and degree of folding through detailed analysis of the magnitude of the current blockade (ΔI) and the associated dwell time (t_d) (figure 1(d)) [10, 13, 24].

While a solid-state nanopore membrane may be based on a single silicon nitride (SiN) [7, 13] or silicon dioxide (SiO_2) [23] layer, more complex designs have been developed with the aim to reduce the electrical noise in nanopore experiments. Minimizing noise is important, because the noise level sets the minimum change in current that can be resolved (i.e. size resolution) at a given filtering frequency (time resolution). Examples of noise-reducing measures include the use of electrically insulating SiO_2 [9, 30] or polymer [25] layers in addition to the thin nanopore membrane. It is important to note that the membrane thickness in the vicinity of the nanopore must remain at the nanometer scale [30] for optimal detection (figure 1(a), bottom red layer). Thus, if the insulating layers are first deposited everywhere on the chip, they must subsequently be removed locally in the region surrounding the nanopore (figure 1(a), top red and blue layers). Typically, this requires a series of time-consuming well-aligned lithography steps. More rapid and simpler means to fabricate nanopore chips with insulating layers locally removed from the region close to the nanopore, would extend the usage of low-noise nanopore chips to a broader range of applications.

In this paper, we present a new fabrication principle, termed *trans*-chip illumination lithography, that addresses this challenge. Our approach relies on using the wafer itself as the lithography mask. When a Si wafer that contains regions of thin membranes (through selective removal of Si) is illuminated from its backside, light is transmitted only through the thin membranes. Hence, photoresist deposited on the top side of the wafer is exposed only in the membrane regions (figure 2). Such local resist exposure can then be used to remove insulating layers exclusively from the membrane regions, without the need of a mask and corresponding alignment steps. By using the membrane features as an intrinsic mask, we avoid time-consuming alignment steps compared to conventional lithography techniques. Furthermore, the fabrication protocol requires only standard fabrication tools and is compatible with four inch-sized wafers, facilitating simultaneous production of multiple (256 in our 4 in. wafer design) nanopore chips and a significant decrease in the process time. We demonstrate the use of *trans*-chip illumination lithography for local removal of insulating layers from nanopore chips containing membranes of different sizes. Using these chips, we investigate and discuss the influences of membrane area and insulating layers on the electrical noise in nanopore experiments. In doing so, we show that the electrical noise of the chips produced in this manner compares favorably to that of chips fabricated without insulating layers.

2. Experimental details

2.1. Definition of free-standing membranes

Our novel *trans*-chip illumination lithography protocol (figure 2 and section 2.2) is applied after conventional fabrication steps have been employed to create a Si wafer patterned with multiple chips, each containing an etched well that exposes a free-standing triple-layer membrane. Here

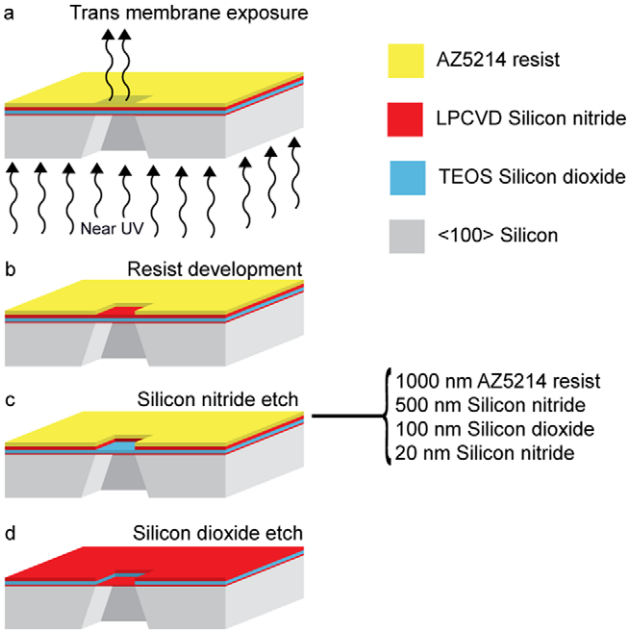

Figure 2. Schematic of *trans*-chip illumination lithography. (a) After forming free-standing triple-layer membranes (SiN, SiO_2, SiN) by conventional fabrication steps, the Si wafer is coated with a resist (AZ5214) layer and illuminated by near-UV light from the backside of the wafer. The resist is locally exposed through the optically transparent triple layer. (b) The exposed resist is removed during development, leaving a square aperture in the resist that has the same width as the underlying free-standing membrane. (c) The SiO_2 layer is laid bare by reactive ion etching of the SiN using a reactive ion etch process. (d) The SiO_2 layer is locally etched using a buffered oxide etch solution, leaving the underlying 20 nm thick SiN membrane intact [32, 33].

we detail the fabrication of the wafer and the free-standing membranes. Both sides of a 4 in. ⟨100⟩ silicon wafer (550 μm thick, single side polished) are coated (by the Delft Institute of Microsystems and Nanoelectronics) with a triple layer [9, 11] consisting of 20 nm silicon nitride by low-pressure chemical vapor deposition (LPCVD SiN), 100 nm tetraethyl orthosilicate silicon dioxide (TEOS SiO_2), and a final layer of 500 nm LPCVD SiN. The unpolished side of the wafer is spin coated with an approximately 1.3 μm thick layer of AZ5214E photoresist (AZ Electronic Materials GmbH, Germany) and patterned using standard optical lithography (EVG620 mask aligner) and MF321 developer (Rohm Haas Electronic Materials). Using reactive ion etching (RIE, 60 min, 50 W, 50 sccm CHF_3 and 2.5 sccm O_2, 8.5 μbar, Leybold) and resist stripping (fuming nitric acid), the triple layer is formed into a mask for potassium hydroxide wet etching (KOH, 400 g l^{-1}, 85 °C).

Seven hours of anisotropic Si wet etching in KOH forms a well in the shape of a pyramidal frustum within each chip (figure 2(a)). As the LPCVD SiN is not etched by KOH [32, 33], the triple layer on the polished side of the wafer remains intact and forms a 620 nm thick free-standing membrane [9, 11]. This triple-layer membrane contains both the final SiN nanopore membrane (figure 2(a), bottom red layer) as well as two thicker insulating layers (figure 2(a), blue and top red layers) [9]. In the same lithography step that defines the wells, a square grid of lines is patterned into the resist to define 256 individual chips on the wafer, as each line in this grid forms a V-shaped groove in the wafer upon KOH etching. The width of the V-shaped grooves (300 μm) was selected to enable manual dicing of the wafer with minimal force (so as to safeguard the free-standing membranes from damage), while simultaneously ensuring that the wafer maintains its structural integrity for the subsequent processing steps.

2.2. Trans-chip illumination lithography and local removal of insulating layers

The 20 nm thick SiN membrane, in which the nanopore is ultimately drilled, is defined by locally removing the two top layers of the triple layer using *trans*-chip illumination lithography (figure 2). After spin coating a 1.3 μm thick resist layer (figure 2(a), yellow layer, AZ5214E, AZ electronic Materials GmbH Germany), the wafer is illuminated from the backside (figure 2(a)) with near-UV light. Because Si is not transparent in this wavelength range, light is only transmitted through the wafer through the optically transparent triple-layer membrane. Light that is transmitted in these regions locally exposes the resist on the top side of the wafer, intrinsically self-aligning the pattern in the resist with the etched wells. A subsequent development step (MF 321, Rohm Haas electronic materials Europe) removes the exposed resist (figure 2(b)).

When the resist-free regions have been defined, removing the 500 nm thick SiN layer (figure 2(c), top red layer) by RIE locally exposes the underlying SiO_2 (figure 2(c), blue layer). Monitoring of the etch process using laser interferometry allows one to determine the exact moment at which the underlying SiO_2 layer is reached. Another 150 s of etching is used to ensure that all the SiN is removed, as the etch rate (20–25 nm min^{-1} in SiN) is known to have spatial inhomogeneities on the scale of a 4 in. wafer. After stripping the resist (fuming nitric acid), the final membrane (figure 2(d), bottom red layer) is obtained by selectively [32, 33] removing the remaining SiO_2 layer on top of the membrane using buffered oxide etch (BHF, AF 87.5–12.5, Aldrich). Note that, during this last step, the 500 nm thick SiN layer acts as a mask for regions beyond the membranes (figure 2(d)). After extensive consecutive rinsing with de-ionized water, acetone, and isopropyl alcohol (IPA) followed by blow drying with nitrogen, the wafer was diced into individual chips. These were stored under vacuum until TEM drilling (Philips CM300UT-FEG or FEI Monochromated Tecnai 200STEM-FEG) of the nanopore at 200 kV. After drilling, the nanopore chips were immediately stored in a 50% ethanol/water mixture until use.

2.3. Nanopore experiment and data recording/analysis

For the electrical noise measurements, the chip containing the nanopore was first rinsed with acetone and ethanol, blown dry, and exposed to an oxygen plasma for around 30 s to enhance the wettability properties of the nanopores. After mounting the chip in a PMMA flow cell and filling both sides of the flow

cell with buffer solution (1 M KCl, 10 mM tris-HCl and 1 mM EDTA, pH 8), Ag/AgCl electrodes were inserted to apply a bias voltage across the nanopore membrane. The ionic current through the nanopore was recorded for 30 s at a bias voltage of 100 mV using an acquisition system (Axon Instruments) consisting of: an Axopatch 200B amplifier, a Digidata 1322A DAQ card and Clampex software. After recording, power spectral density spectra (PSD) of the data traces were created using Clampfit software (Axon Instruments).

3. Results and discussion

We used scanning electron microscopy (SEM) to examine the finalized membrane chips (figure 3). Imaging the top side of a chip head on (figure 3(b)), we observe a difference in contrast between the etched region and the surrounding chip. When imaged at higher resolution under an angle of 30° (figure 3(c)), a difference in topology between the etched region and the surrounding chip becomes visible: the wall of the etched region is clearly discernible, and the separate SiO_2 and SiN layers can even be identified through a subtle difference in contrast (figure 3(f)). Hence, it is clear from the SEM images that the insulating layers have been successfully removed from, and only from, the membrane regions. However, while the aperture in the Si has sharp corners, as clearly visible upon imaging the chip from its back side (the well side, figure 3(d)), the corners of the square etched into the insulating layers are somewhat rounded, with a radius of curvature of ∼500 nm (figures 3(b) and (c)). Using high magnification to image the corner alone (figure 3(c)), we also observe that the neighboring walls display a wavy pattern that extends around 2 μm beyond the corner. We attribute the formation of these patterns and the rounded corners to the diffraction of light at the sharp corners of the aperture [7] in the underlying Si.

To ensure the most reproducible transfer of the 'mask' pattern into the photoresist, using *trans*-chip illumination, we found it necessary to tune the exposure time of the resist. When the chips were exposed using the resist's standardized exposure time (7 s@12 mW cm^{-2}), the insulating layers were only removed from a fraction of the membranes, indicating that the resist must not have been fully removed from all membrane regions prior to etching. This lack of resist removal most likely results from under-exposure of the resist, which can be explained by light losses in the membrane through absorption [6] and scattering [7]. With an increased exposure time of 14 s (figure 3(e)), the insulating layers were successfully removed from all membranes that were examined, indicating that the resist was properly exposed and developed throughout the wafer. Even longer exposure times were not more favorable, as they resulted in an increasingly wider etched pattern compared to the size of the rectangular aperture in the underlying silicon wafer (figures 3(c), (e) and (g)). This broadening is explained by the fact that at longer exposure times, a larger part of the diffraction pattern [7] exceeds the damage threshold of the photoresist. This is in agreement with a more pronounced wavy pattern in the wall of the etched region at longer exposure times (figures 3(c), (e) and (g)). To ensure proper structuring of the resist on all 256 chips on the wafer we adopted an exposure time of 14 s throughout the rest of the study.

Table 1. The dimensions and properties of the 20 nm thick SiN membranes for the five different chip designs (figure 4) used in this study, as measured by scanning electron microscopy.

Design nr.	Insulating SiO_2 and SiN layers	Dimension of the SiN membrane
1	No	65 μm × 65 μm
2	No	12 μm × 12 μm
3	Yes	65 μm × 65 μm
4	Yes	12 μm × 12 μm
5	Yes	5 μm diameter circle within 65 μm × 65 μm triple layer

With the *trans*-chip illumination lithography protocol in hand, we studied the effect of membrane size and the presence or absence of electrically insulating layers on the noise in nanopore experiments. Four chip designs were fabricated (figure 4 and table 1) in which we varied the width of the membrane as well as the presence of the insulating layers beyond the membrane region. For the largest area membrane (figure 4(a), design 1), we selected an area of 65 μm × 65 μm, because membranes of this size are sufficiently stable for use in nanopore experiments and can be fabricated in a reproducible manner. For the smallest area membrane (figure 4(a), design 2, red layer), we aimed for an area of 10 μm × 10 μm. In practice, after etching through the 550 μm thick wafers the windows for the chips that were employed had areas of 12 μm × 12 μm due to variations in the etching process. To study the effect of insulating layers on the electrical noise, we fabricated chips with and without insulating layers for both of these membrane sizes. To avoid any potential influence from variations in the raw material on the noise characteristics of the various designs, we fabricated all designs (figure 4(a)) starting from identical wafers. Chips with insulating layers (figure 4(a), design 3, 65 μm×65 μm; figure 4(a), design 4, 12 μm×12 μm) were prepared via *trans*-chip illumination lithography. For chips without insulating layers (figure 4(a), designs 1 and 2), the application of resist and *trans*-chip illumination lithography steps was omitted, and hence the SiN and SiO_2 layers were removed over the entire surface of the chip during the etching procedures. In the noise analysis we also compare our new designs with chips that were fabricated using our previously described, more elaborate, approach, which relies on electron beam lithography to form a 5 μm wide circular SiN membrane in a 65 μm × 65 μm free-standing triple-layer membrane (figure 4(a), design 5) [9].

After drilling a nanopore into each membrane using a transmission electron microscope (TEM), [26] we performed electrical noise measurements for each design using an Axopatch amplifier. For the research presented here, we only used circularly shaped pores (figure 1(b)) with a diameter of 20 ± 1 nm [26, 23], as determined by TEM. Additionally, by using a beam size of ∼10 nm (smaller than the pore to be drilled), we ensured that the nanopores all had similar profiles that closely resembled a cylinder [26]. To avoid

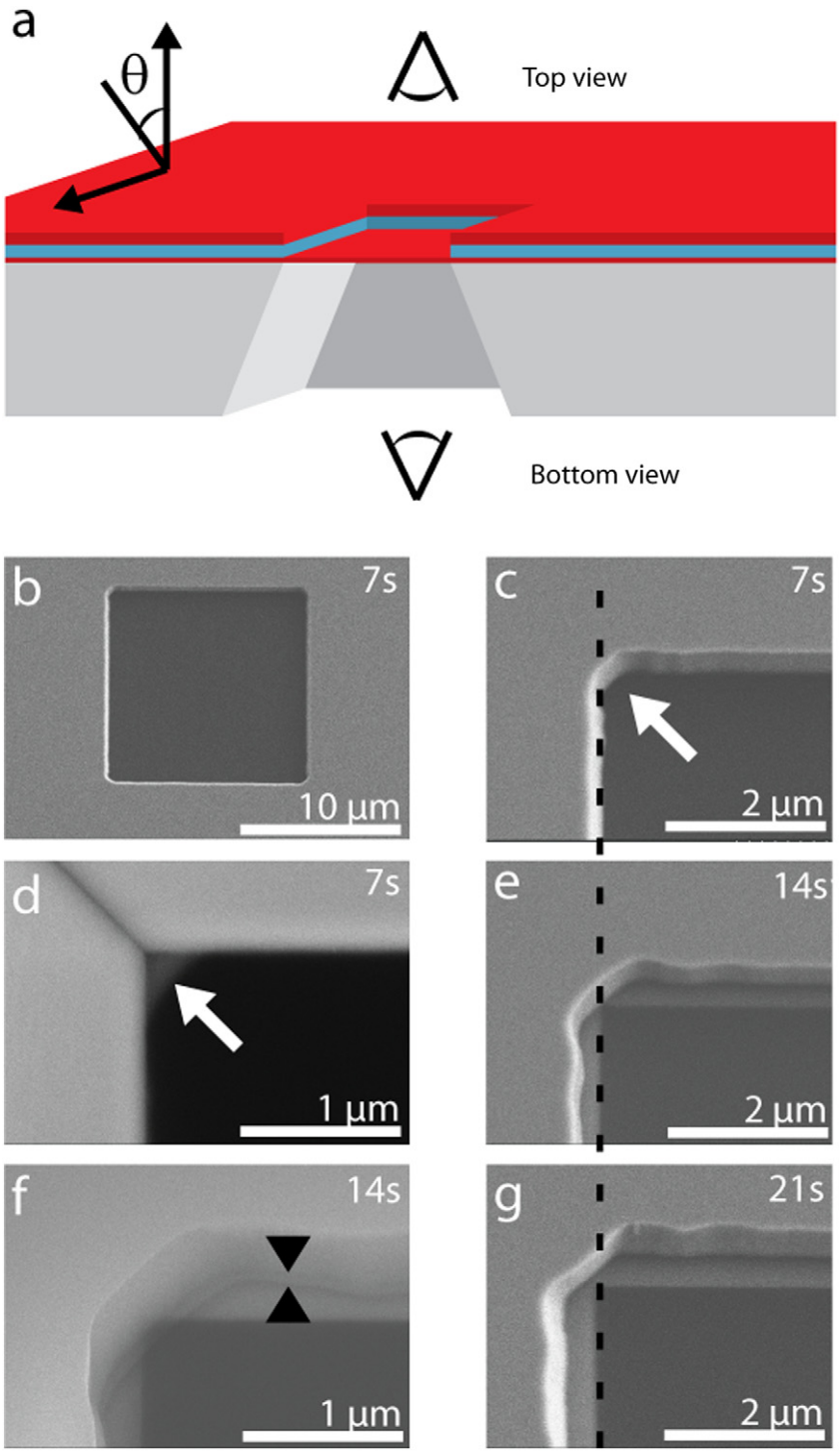

Figure 3. SEM analysis of *trans*-chip illumination lithography membranes. (a) Schematic representation of the final free-standing silicon nitride membrane (cross section and not to scale) and the SiN and SiO_2 insulating layers. (b)–(g) The 20 nm thick free-standing SiN membranes (12 μm × 12 μm) shown in the SEM pictures are manufactured according to the procedure described in figure 2. The duration of the near-UV exposure is indicated in the individual images. (b) Top view shows the sharp definition of the square membrane after *trans*-chip illumination lithography and etching of the insulating layers. (c) High-magnification SEM image (top view with $\theta = 30°$) of the top-left corner of the picture in panel (b). The rounded corner of the etched SiN and SiO_2 layers has a radius of curvature of ∼500 nm (white arrow). (d) In the bottom view of the chip, the well in the Si shows a square corner while the rounded corner of the (now underlying) SiO_2 and SiN (white arrow) is visible through the 20 nm thick SiN membrane. (e) Increasing the exposure time from 7 to 14 s makes the etched aperture in the insulating layers larger than the underlying square well in the Si wafer as a larger part of the diffraction pattern exceeds the threshold of the photoactive resist upon increasing the exposure time [7]. For clarity, the edge of the square silicon well is aligned (dashed line) in panels (c), (e) and (g) (all imaged from the top side with $\theta = 30°$). The wavy and symmetric diffraction patterns are clearly visible around the sharp corner of the Si well. (f) Close-up of the corner shows the presence of the SiO_2 layer (between black arrows) between the SiN top layer and the SiN membrane (imaged from the top side with $\theta = 30°$). (g) Further increase of the exposure time increases the over-exposure of the pattern (imaged from the top side with $\theta = 30°$).

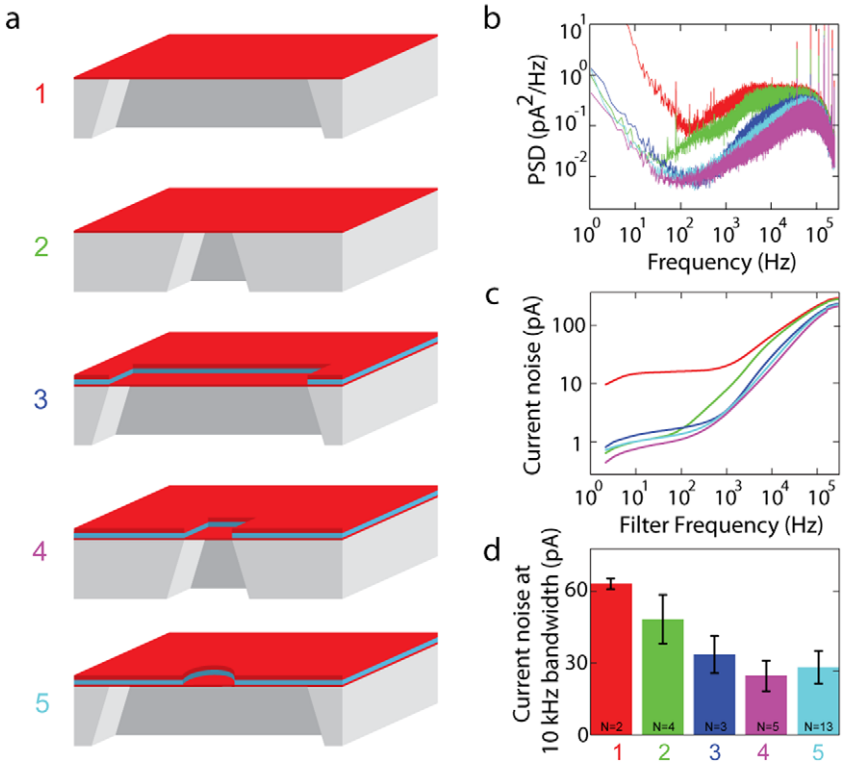

Figure 4. The effect of membrane geometry and presence of insulating layers on noise. (a) Schematic representation of the various membrane geometries used to study the influence of geometry on noise. The designs are indicated by a color-coded number and the same color coding is used in panels (b)–(d). The designs (1–4) in which we varied the size of the membrane and the presence of insulation layers (SiO_2 and SiN) are fabricated by *trans*-chip illumination lithography, whereas design number 5 is fabricated using a more elaborate approach that relies on electron beam lithography [9]. (b) Power spectral density (PSD) spectra for the different designs measured at 100 mV using 20 nm nanopores drilled into the 20 nm thick silicon nitride membranes. At low frequency (<100 Hz), the PSD decreases as $1/f^{\alpha}$ with increasing frequency. At high frequency (>100 Hz), the noise is dictated by capacitive noise [19, 20, 25]. The distinct peaks in the spectra at high frequency ($>10^5$ Hz) are caused by the patch clamp amplifier's electronics and are unique to each individual setup. Note that for simplicity, we have here plotted, for each design, the individual PSD spectrum of the chip demonstrating the lowest $1/f^{\alpha}$ noise. (c) The square root of the individual PSD spectra of panel (b) integrated over frequency to give the cumulative current noise up to a given filter frequency. (d) The cumulative current noise (square root of the integrated PSD) up to 10 kHz for the various geometries averaged over several measurements. These individual measurements were performed on individual chips to show the reproducibility of the measurements. The error bars represent the standard deviation measured for these N measurements.

possible variation in noise from differences in experimental conditions, all measurements were performed on the same instrumental setup. Unless otherwise mentioned, all results represent averages of multiple measurements on multiple pores.

We can quantify the electrical noise by examining the typical overall shape of the measured power spectral density (PSD) spectra, which for the different designs exhibits the characteristic frequency dependence reported in previous studies on bare SiN and coated SiN membranes (individual PSD spectra are shown figure 4(b); same color code employed as in figure 4(a)) [19, 20, 25]. Specifically, at low frequency (f < 100 Hz) the PSD decreases with $1/f^{\alpha}$, [25] while above 100 Hz, the noise increases as the contribution due to the capacitance of the chip becomes dominant. At very high frequency (f > 100 kHz) the measured PSD decreases due to the internal filters present in the amplifier employed (figure 4(b)). For each design, the low frequency $1/f^{\alpha}$ noise can vary by up to two orders of magnitude between chips fabricated in the same manner, a behavior that has also been observed by other groups [25, 3–5]. Various physical effects have been invoked to explain the origin of the low frequency $1/f^{\alpha}$ noise [25], including surface effects [3, 5, 16], motion of charged constituents on the nanopore wall [17, 1, 2], and the formation of nanobubbles [18]. For simplicity, we have here plotted the PSD spectrum of the chip demonstrating the lowest $1/f^{\alpha}$ noise for each of the five designs (figures 4(b) and (c)), whilst the final characterization and comparison of the designs relies on results that are averaged over multiple chips and measurements (figure 4(d)). The high-frequency noise that results from the chip's capacitive behavior [25, 20, 12, 22] is found to be more reproducible between chips of the same design and is comparable with the noise levels reported in literature [25, 19, 20] for both bare and coated chips. The distinct peaks in the spectra at high frequency are caused by the patch clamp amplifier's electronics and are unique for each measurement setup. By comparing the PSD spectra for the different membrane designs, it becomes clear that a small membrane size in combination with insulating layers (design 4) yields the best result regarding noise over the entire frequency range (figure 4(b), the purple curve falls below all other curves over the entire frequency range).

To further compare the different nanopore chip designs, we compared their cumulative noise integrated from 0 Hz up to a given filtering frequency (f_{filter}). The cumulative noise is experimentally relevant as it measures the experimentally observed noise level at that filtering frequency. We furthermore take the square root of the integrated PSD spectrum to yield the current noise (as opposed to the power noise). Figure 4(c) shows the current noise plotted as a function of f_{filter}. Since the noise measurements are performed with no additional filtering beyond the 100 kHz internal filter of the amplifier, such a plot allows us to compare the performance of the different designs at different filter frequencies (time resolutions). For example, it is clear from figure 4(c) that the smallest membrane together with insulating layers (design 4) provides the lowest noise independent of filtering frequency, although the difference compared with the larger membrane with insulating layers (design 3) or our previous more elaborate design (design 5) is small at intermediate frequencies ($f_{\text{filter}} \approx 1$ kHz).

To compare the various designs at filtering frequencies commonly used in nanopore experiments, we measured the integrated current noise at $f_{\text{filter}} = 10$ kHz (corresponding to a time resolution of 100 μs, sufficient to resolve the typical $\sim$1 ms dwell time of a current blockade (figure 1(d))) and averaged over multiple individual chips for each design (figure 4(d)). Independent comparisons of the noise values for the small membranes (comparing design 2 and 4) and the large membranes (comparing design 1 and 3) quantitatively shows that the presence of the insulating layers decreased the current noise by a factor 2.2 ± 0.1, independent of the size of the membrane. Reduction of the membrane size from 4225 to 144 μm^2 (compare designs 1 and 2, or designs 3 and 4) also reduces the current noise, but to a lesser extent: a factor of 1.4 ± 0.1. These results can be understood from the capacitive contribution to the noise [12, 25], which originates not only from the capacitance of the thin membrane separating the two saline compartments but also from the capacitance between the Si chip and the saline solution. To understand the capacitance effect between the Si and the solution, it must be realized that, during a nanopore experiment, the Si wafer is in contact with the saline solution via the exposed walls of the pyramidal well. Consequently, the Si of the chip is at the same electrical potential as the liquid (figures 1(a) and (c)) and separated from the other fluid compartment by the 20 nm thick insulating SiN layer on top of the chip. Increasing the thickness of this insulating layer through the addition of insulating SiO_2 and SiN layers (compare designs 1 and 3, or designs 2 and 4) decreases the capacitance, which in turn, results in a lower noise [12, 25]. Similarly, reducing the area of the 20 nm thick SiN membrane itself (i.e. the aperture in the Si chip: compare designs 1 and 2, or designs 3 and 4) reduces the chip's capacitance and hence the electrical noise.

The current noise measured for design 5 is situated midway between that of new designs 3 and 4 (figure 4(d)). This can be understood by comparing the three geometries in more detail. First, while the apertures in the Si of designs 3 and 5 are identical (4225 μm^2), the areas of the 20 nm thick SiN membrane differ between the two designs. In design 3, the thin membrane is 4225 μm^2, whereas it is only 20 μm^2 in design 5 (area of the circular pattern) as the insulating SiO_2 and SiN layers partially cover the 4225 μm^2 aperture. Consequently, the capacitance and by that the noise of design 5 is lower than that of design 3. Comparing design 5 with design 4 we note that the area of the 20 nm thick SiN membrane is smaller for design 5 (20 μm^2 versus 144 μm^2). However, design 5 has a much larger aperture in the Si (4225 μm^2) than design 4 (144 μm^2). The noise increase that results from the larger free-standing SiN membrane (144 μm^2 versus 20 μm^2) of design 4 is more than compensated by the decrease of noise due to the smaller aperture in the silicon (144 μm^2 versus 4225 μm^2). In conclusion, the presence of insulating layers as well as reduction of the membrane area reduces the electrical noise in nanopore chips. Trans-illumination lithography is ideal in this respect, as it allows for straightforward removal of the insulating layers from, and only from, the membrane, independently of membrane size.

4. Conclusions

We have introduced a novel method for the rapid production of low-noise, free-standing membranes for nanopore experiments. Our new approach is based on exposing a photoresist (on the top side of a wafer) from the backside of the wafer, such that previously defined structures in the wafer take on the role of the lithography mask. This obviates the need for a separate mask and accompanying alignment steps. In fact, the procedure can be performed without mask aligner. Effectively, we have not only decreased the patterning time for local removal of the insulating layers, but through the inherent self-aligning property of *trans*-chip illumination lithography we have also simplified the fabrication protocol and rendered it less error prone. The rate-limiting step in the current production process is the nanopore drilling by TEM, because the chips are loaded and drilled individually. Ultimately, we envision that our new manufacturing protocol will be combined with novel drilling techniques capable of rapid drilling of nanopores on a wafer-wide scale [15, 34] compared to the chip-by-chip drilling by TEM.

By direct comparison of nanopore chips of different designs we have shown that the electrical noise is significantly reduced by the presence of insulating layers and to a lesser extent by reduction of the size of the membrane. *Trans*-chip illumination lithography is highly suited for fabrication of such chips, because it allows one to preferentially remove insulating layers from the free-standing membrane. Importantly, we have demonstrated that nanopore chips fabricated by *trans*-chip illumination lithography have comparable electrical noise characteristics to more elaborate chip designs that require time-consuming, error prone, and costly fabrication.

Finally, we note that the *trans*-chip illumination lithography can potentially find wide application in other research fields. For example, the self-alignment principle could be used also to deposit (instead of remove)

materials preferentially in the regions of thin membranes. Further, negative photoresists may be used to modify regions that surround membranes without modifying the membranes themselves. Based on its simplicity and the numerous possibilities it offers, we anticipate that *trans*-chip illumination lithography will be useful both for solid-state nanopore fabrication as well as for other applications, e.g. fabricating thin free-standing membranes or structure resist on locally transparent substrates.

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References

[1] Banerjee J, Verma M K, Manna S and Ghosh S 2006 Self-organised criticality and 1/*f* noise in single-channel current of voltage-dependent anion channel *Europhys. Lett.* **73** 457–63

[2] Bezrukov S M and Winterhalter M 2000 Examining noise sources at the single-molecule level: 1/*f* noise of an open maltoporin channel *Phys. Rev. Lett.* **85** 202–5

[3] Chen P, Mitsui T, Farmer D B, Golovchenko J, Gordon R G and Branton D 2004 Atomic layer deposition to fine-tune the surface properties and diameters of fabricated nanopores *Nano Lett.* **4** 1333–7

[4] Collins P G, Fuhrer M S and Zettl A 2000 1/*f* noise in carbon nanotubes *Appl. Phys. Lett.* **76** 894–6

[5] Danelon C, Perez J B, Santschi C, Brugger J and Vogel H 2006 Cell membranes suspended across nanoaperture arrays *Langmuir* **22** 22–5

[6] Deshpande S V, Gulari E, Brown S W and Rand S C 1995 Optical-properties of silicon–nitride films deposited by hot-filament chemical-vapor-deposition *J. Appl. Phys.* **77** 6534–41

[7] Jung Y, Vacic A, Sun Y, Hadjimichael E and Reed M A 2012 Mapping of near field light and fabrication of complex nanopatterns by diffraction lithography *Nanotechnology* **23** 045301

[8] Kasianowicz J J, Brandin E, Branton D and Deamer D W 1996 Characterization of individual polynucleotide molecules using a membrane channel *Proc. Natl Acad. Sci. USA* **93** 13770–3

[9] Keyser U F, Krapf D, Koeleman B N, Smeets R M M, Dekker N H and Dekker C 2005 Nanopore tomography of a laser focus *Nano Lett.* **5** 2253–6

[10] Kowalczyk S W, Hall A R and Dekker C 2010 Detection of local protein structures along DNA using solid-state nanopores *Nano Lett.* **10** 324–8

[11] Krapf D, Wu M Y, Smeets R M M, Zandbergen H W, Dekker C and Lemay S G 2006 Fabrication and characterization of nanopore-based electrodes with radii down to 2 nm *Nano Lett.* **6** 105–9

[12] Levis R A and Rae J L 1993 The use of quartz patch pipettes for low-noise single-channel recording *Biophys. J.* **65** 1666–77

[13] Li J, Gershow M, Stein D, Brandin E and Golovchenko J A 2003 DNA molecules and configurations in a solid-state nanopore microscope *Nature Mater.* **2** 611–5

[14] Li J, Stein D, McMullan C, Branton D, Aziz M J and Golovchenko J A 2001 Ion-beam sculpting at nanometre length scales *Nature* **412** 166–9

[15] Marshall M M, Yang J and Hall A R 2012 Direct and transmission milling of suspended silicon nitride membranes with a focused helium ion beam *Scanning* **34** 101–6

[16] Nilsson J, Lee J R I, Ratto T V and Letant S E 2006 Localized functionalization of single nanopores *Adv. Mater.* **18** 427–31

[17] Siwy Z and Fulinski A 2002 Origin of 1/*f* (alpha) noise in membrane channel currents *Phys. Rev. Lett.* **89** 158101

[18] Smeets R M, Keyser U F, Krapf D, Wu M Y, Dekker N H and Dekker C 2006 Salt dependence of ion transport and DNA translocation through solid-state nanopores *Nano Lett.* **6** 89–95

[19] Smeets R M M, Dekker N H and Dekker C 2009 Low-frequency noise in solid-state nanopores *Nanotechnology* **20** 095501

[20] Smeets R M M, Keyser U F, Dekker N H and Dekker C 2008 Noise in solid-state nanopores *Proc. Natl Acad. Sci. USA* **105** 417–21

[21] Smeets R M M, Keyser U F, Krapf D, Wu M Y, Dekker N H and Dekker C 2006 Salt dependence of ion transport and DNA translocation through solid-state nanopores *Nano Lett.* **6** 89–95

[22] Steinbock L J, Otto O, Chimerel C, Gornall J and Keyser U F 2010 Detecting DNA folding with nanocapillaries *Nano Lett.* **10** 2493–7

[23] Storm A J, Chen J H, Ling X S, Zandbergen H W and Dekker C 2003 Fabrication of solid-state nanopores with single-nanometre precision *Nature Mater.* **2** 537–40

[24] Storm A J, Chen J H, Zandbergen H W and Dekker C 2005 Translocation of double-strand DNA through a silicon oxide nanopore *Phys. Rev.* E **71** 051903

[25] Tabard-Cossa V, Trivedi D, Wiggin M, Jetha N N and Marziali A 2007 Noise analysis and reduction in solid-state nanopores *Nanotechnology* **18** 305505

[26] van den Hout M, Hall A R, Wu M Y, Zandbergen H W, Dekker C and Dekker N H 2010 Controlling nanopore size, shape and stability *Nanotechnology* **21** 115304

[27] van den Hout M, Krudde V, Janssen X J A and Dekker N H 2010 Distinguishable populations report on the interactions of single DNA molecules with solid-state nanopores *Biophys. J.* **99** 3840–8

[28] van den Hout M, Skinner G M, Klijnhout S, Krudde V and Dekker N H 2011 The passage of homopolymeric RNA through small solid-state nanopores *Small* **7** 2217–24

[29] Wanunu M, Bhattacharya S, Xie Y, Tor Y, Aksimentiev A and Drndic M 2011 Nanopore analysis of individual RNA/antibiotic complexes *ACS Nano* **5** 9345–53

[30] Wanunu M, Dadosh T, Ray V, Jin J M, McReynolds L and Drndic M 2010 Rapid electronic detection of probe-specific microRNAs using thin nanopore sensors *Nature Nanotechnol.* **5** 807–14

[31] Wanunu M, Sutin J and Meller A 2009 DNA profiling using solid-state nanopores: detection of DNA-binding molecules *Nano Lett.* **9** 3498–502

[32] Williams K R, Gupta K and Wasilik M 2003 Etch rates for micromachining processing—part II *J. Microelectromech. Syst.* **12** 761–78

[33] Williams K R and Muller R S 1996 Etch rates for micromachining processing *J. Microelectromech. Syst.* **5** 256–69

[34] Yang J, Ferranti D C, Stern L A, Sanford C A, Huang J, Ren Z, Qin L-C and Hall A R 2011 Rapid and precise scanning helium ion microscope milling of solid-state nanopores for biomolecule detection *Nanotechnology* **22** 285310